REMARKS

Applicant respectfully requests reconsideration of the present application in view of the reasons that follow.

A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

No claims have been amended. Claims 1-31 remain pending in this application, of which claims 25-31 are withdrawn from consideration.

Allowable subject matter

Applicants appreciate the indication that claims 14-24 are allowed and claims 2-3, 5-6 and 8-9 contain allowable subject matter.

Rejection under 35 U.S.C. § 102

Claims 1, 4, 7 and 10-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,760,644 to Lancaster et al. ("Lancaster"). Applicants respectfully traverse this rejection for at least the following reasons.

Independent claim 1 is directed to a time limit function utilization apparatus, and comprises a semiconductor time switch which is interposed in or connected to the signal line (which connects a first functional block and a second functional block), and substantially disables or substantially enables mutual access between the first functional block and second functional block upon a lapse of a first predetermined time. Lancaster fails to disclose or suggest at least this feature of claim 1.

Lancaster discloses a timer 30 including a dielectric 20 in which charge 32 is trapped, a voltage measurement circuit 100, and a charge injection circuit 101 (Figure 1, col. 3, lines 57-62). Lancaster also discloses:

> The timer/clock integrated circuit can be . . . embedded in an integrated circuit where additional circuitry can augment the functionality of the invention, or the invention can augment the functionality of other circuitry. For example, with the addition of non-volatile registers and computational circuits, a real

> time clock calendar can be constructed. Or when embedded in a memory, the timer can be used to trigger a refresh operation whenever power is available. (col. 2, lines 20-27).

In contrast to the semiconductor time switch as recited in claim 1, however, Lancaster does not disclose that his timer 30 is interposed in or connected to a signal line, which connects a first functional block and a second functional block, and substantially disables or substantially enables mutual access between the first functional block and second functional block. Specifically, Lancaster does not disclose that the timer 30 connects two functional blocks in order to allow mutual access between the functional blocks. While Lancaster discloses that the timer 30 may be embedded in other circuitry, Lancaster does not disclose any embodiment where the timer 30 connects two functional blocks in order to allow mutual access between the blocks.

While Lancaster does disclose that the timer may be embedded in a memory, where the timer can be used to trigger a refresh operation whenever power is available, Lancaster does not suggest in this context that the timer disables or enables mutual access between first and second functional blocks, even if the memory elements could be considered to be a functional block and any power source to the memory elements to be another functional block. Lancaster merely discloses that the timer 32 triggers a refresh operation, and does not disable or enable mutual access between any first and second functional blocks.

The claims ultimately depending from claim 1 are patentable for at least the same reasons, as well as for further patentable features recited therein. For example, Lancaster does not disclose all the features of dependent claim 7. The Office Action appears to equate elements 301 and 302 of Lancaster with the "other terminal" of claim 7, which is connected to the third functional block, and the first input/ouput terminal, respectively. Element 301, however, is a gate electrode and is not "the other terminal of the semiconductor time switch" recited in claim 7. In contrast to claim 7, there is no time switch provided between source 302 and gate 301 of Lancaster which would function in the manner recited in claim 7. Presuming for the sake of argument that the transistor of Figure 3 in Lancaster could be considered a time switch, the terminals of such a switch would correspond to source 302 and drain 303, respectively, not source 302 and gate 301. Lancaster, however, does not disclose the three functional blocks arranged relative to the terminals in the manner recited in claim 7.

Dependent claim 11 recites "by supplying charges to the gate electrode in advance." By contrast, Lancaster discloses only storing charge in nitride 32', not in a gate electrode, which would correspond to the poly gate of Lancaster.

Dependent claim 12 recites the charges are injected into or leak from a gate electrode via a semiconductor or Schottky junction. By contrast, Lancaster does not disclose injecting charges into its nitride via a semiconductor or Schottky junction. The "NPN junction" of Lancaster referred to in the Office Action with respect to claim 12, is part of the transistor 31' itself, not a separate junction that injects charge into nitride 32 of Lancaster's transistor 31'.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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By

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